REMARKS

The Office Action mailed on February 2, 2006, as well as the art cited, has been reviewed. Claims 1-6, 9-19, and 22-26 are pending in this application.

Double Patenting Rejection

Claims 1-6, 9-19, and 22-26 were rejected under a non-statutory obviousness-type double patenting rejection, specifically U.S. Patent No. 6,678,836 B2. A Terminal Disclaimer in compliance with 37 CFR 1.321(c) is enclosed herewith to overcome this rejection.

Rejections Under 35 U.S.C. § 102

Claims 1, 10, 13, 14, 23, and 26 are rejected under 35 USC § 102(b) as being anticipated by Douceur (U.S. Patent No. 5,838,893). Applicant respectfully traverses this rejection.

Applicable Law

35 U.S.C. §102 provides in relevant part:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

A claim is anticipated under 35 U.S.C.§ 102 only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference. *Verdegaal Bros. v. Union Oil Co. of California,* 814 F.2d 628, 631, 2 U.S.P.Q.2d 1051, 1053 (Fed. Cir. 1987). "The identical invention must be shown in as complete detail as is contained in the . . . claim." *Richardson v. Suzuki Motor Co.,* 868 F.2d 1226, 1236, 9 U.S.P.Q.2d 1913, 1920 (Fed. Cir. 1989). The elements must be

arranged as required by the claim, but identical terminology is not required. *In re Bond*, 910 F. 2d 831, 15 U.S.P.Q.2d 1566 (Fed. Cir. 1990).

Anticipation focuses on whether a claim reads on a product or process disclosed in a prior art reference, not on what the reference broadly teaches. *Kalman v. Kimberly-Clark Corp.*, 713 F.2d 760, 218 U.S.P.Q. 781 (Fed. Cir. 1983). To anticipate a claim, a reference must disclose every element of the challenged claim and enable one skilled in the art to make the anticipating subject matter. *PPG Industries, Inc. v. Guardian Industries Corp.*, 75 F.3d 1558, 37 U.S.P.Q.2d 1618 (Fed. Cir. 1996).

Claims 1, 10 and 13

Claim 1 is as follows (emphasis added):

1. A method for remapping locations in memory, comprising:

generating a remapping value;

logically combining the remapping value with an intended address value to generate a remapped address value, wherein one or more bad memory address values exist and wherein the remapping value is logically combined with only intended address values that equal one of the bad memory address values to generate a remapped address value for only the one or more bad memory address values; and

accessing a memory location having the remapped address value.

Applicant respectfully asserts that Douceur does not teach or suggest the method of claim 1. Douceur does not describe "wherein the remapping value is logically combined with only intended address values that equal one of the bad memory address values to generate a remapped address value for only the one or more bad memory address values." Douceur does discuss "a method and system for remapping physical memory addresses so that the physical memory addresses of bad memory locations are in the high physical memory addresses." (*See* Douceur, Col. 3, lines 55-58). However, the remapping of Douceur differs significantly from the remapping called for in the method of claim 1.

As discussed previously, Douceur re-maps *all* addresses rather than remapping only the bad addresses. (*See* Preliminary Amendment filed Nov 18, 2003, pg. 1). This difference between claim 1 of the present application and the disclosure of Douceur is illustrated in Douceur's Fig. 4. Fig. 4 is reproduced below:

CPU	mem
0000	1010
0001	1011
0010	1000
0011	1001
0100	1110
0101	1111
0110	1100
0111	1101
1000	0010
1001	0011
1010	0000
1011	0001
1100	0110
1101	0111
1110	0100
1111	0101

Fig. 4

In discussing Fig. 4, Douceur explains at Col. 4, lines 30-45:

FIG. 4 contains a table that illustrates the remapping of the physical memory addresses. When the bits 0000 are exclusive-ORed with the bits 1010 of the remapping value, the result is bits 1010. Of particular interest is that the bits 0101, which correspond to the highest-order bits of the lowest address and highest address

> in the range, when exclusive-ORed with the bits 1010 result in the bits 1111. The bits 1111 result in selecting the highest physical memory addresses. Thus, any physical memory address in the range from the lowest address to the highest address is mapped to high physical memory address. Thus, the contiguous area of physical memory below the remapped lowest address is now available. The system also sets the memory size 305 by setting the number of highest-order bits (e.g., 4) to 1 and then setting the lowest-order bits to the lowest-order bits of the lowest address of the range. Thus, the highest available address is just below the remapped lowest address.

Fig. 4 of Douceur shows that *all* addresses are remapped. The left-hand column of Fig. 4 includes the four highest-order bits of addresses received from the CPU. The right-hand column is the result of the XOR of these bits with the remapping value and thus is the highest order bits of the remapped address. As Applicant pointed out previously, the example continues in Fig. 5 showing addresses of page 0 (0000) being mapped to page 10 (1010). (*See* Douceur, Fig. 4, Row 1). When viewed in isolation, Applicant can understand why the Examiner was confused in stating that "[t]he Examiner could not find in the specification where page 0 and 10 are good pages." (*See* Office Action, pg. 9). However, when reading the example as a whole and viewing Figs. 3, 4, and 5 of Douceur together, it is clear that Douceur illustrates application of the remapping value to all 15 pages. It is true that Douceur did not explicitly say that pages 0-4 and 6-15 were good; however, Applicant respectfully asserts that it is inherent from the totality of the example that these pages are good. If Applicant is to take the Examiner's assumption from Fig. 5 of Douceur that remapping is applied *only* to bad memory locations, the Applicant would have to conclude *all* memory locations are bad because Fig. 4 of Douceur shows the remapping value applied to *all* pages of the memory. This could not be a correct reading of the example of Douceur. Therefore, Applicant respectfully contends that the correct reading of the example of Douceur is that Douceur applies the remapping value to *all* addresses (the bad and good memory address values), even though Fig. 5 of Douceur only explicitly shows some of the remapping.

There is no teaching or suggestion in Douceur to generate a remapped address value for *only* the one or more bad memory address values, wherein the remapping value is logically combined with *only* intended address values that equal one of the bad memory address values. Rather, the discussion of the various elements in the method contemplated by Douceur above makes it very clear that *all* memory locations are remapped, not just the bad memory locations, without regard to the condition of memory at a particular memory address.

In summary, Douceur neither discloses nor suggests logically combining the remapping value with an intended address value to generate a remapped address value, wherein one or more bad memory address values exist and wherein the remapping value is logically combined with only intended address values that equal one of the bad memory address values to generate a remapped address value for only the one or more bad memory address values as found in claim 1. Accordingly, it is respectfully requested that the rejection of claim 1 be withdrawn.

Claims 10 and 13 depend from claim 1. Accordingly, it is respectfully requested that the rejection of these claims be withdrawn for at least the same reasons as claim 1.

Claims 14, 23 and 26

Claim 14 is as follows (emphasis added):

14. A system for remapping locations in memory, comprising:

a first logic for outputting a remapping value;

a second logic configured to combine the remapping value with an intended address value to generate a remapped address value, wherein one or more bad address values exist and wherein the second logic combines the remapping value with only the intended address value that equals one of the bad memory address values to generate a remapped address value for only the one or more bad memory address values; and

a memory address input configured to access a memory location having the remapped address value.

Applicant respectfully asserts that Douceur does not teach or suggest the system of claim 14. Applicant refers the Examiner to the arguments presented above with respect to claim 1. As discussed above, Douceur discloses "a method and system for remapping physical memory addresses so that the physical memory addresses of bad memory locations are in the high physical memory addresses." (*See* Douceur, Col. 3, lines 55-58). Douceur does not teach or suggest remapping *only* addresses associated with bad memory address values.

As discussed above with respect to claim 1, there is no teaching or suggestion in Douceur to combine the remapping value with an intended address value to generate a remapped address value, wherein one or more bad address values exist and wherein the second logic combines the remapping value with only the intended address value that equals one of the bad memory address values. Rather, the discussion of the various elements in the system contemplated by Douceur makes it very clear that *all* memory locations are remapped, not just the bad memory locations, without regard to the condition of memory at a particular memory address.

In summary, Douceur neither discloses nor suggests a second logic configured to combine the remapping value with an intended address value to generate a remapped address value, wherein one or more bad address values exist and wherein the second logic combines the remapping value with only the intended address value that equals one of the bad memory address values to generate a remapped address value for only the one or more bad memory address values as found in claim 14. Accordingly, it is respectfully requested that the rejection of claim 14 be withdrawn.

Claims 23 and 26 depend from claim 14. Accordingly, it is respectfully requested that the rejection of these claims be withdrawn for at least the same reasons as claim 14.

Rejections Under 35 U.S.C. § 103

Claims 12 and 25 were rejected under 35 USC § 103(a) as being unpatentable over Douceur ('893) as applied to claims 1 and 14 above, and in further view of Logic and Computer Design, by Mano et al. Applicant respectfully traverses this rejection.

Applicable Law

35 U.S.C. §103 provides in relevant part:

> Conditions for patentability; non-obvious subject matter.
>
> (a) a patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

To establish a case of *prima facie* obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art and not based in the applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir 1991). MPEP § 2143 - § 2143.03.

Claim 12

Claim 12 depends from independent claim 1. As a result, the arguments presented above with respect to claim 1 apply to this claim as well. Claim 12 further defines the method of claim 1 wherein the remapping value and the intended address value are exclusively-NORed to produce the remapped address value.

The Office Action took the position that while "Douceur discloses that the system applies the remapping value to the received address by performing a bitwise exclusive-OR of the bits of the received address with the bits of the remapping value", it fails to "explicitly disclose using an exclusive-NOR to reproduce the remapping address value." The Office Action indicated that Mano et al. discloses this feature. The Office Action then concluded that "It would have been obvious to one of ordinary skill at the time of the invention to include the exclusive-NOR of Mano et al. into the system of Douceur. A person of ordinary skill in the art would have been motivated to make the modification because an XOR and XNOR gate can be used interchangeably since one is just the complement of the other (see Mano et al, page 78). Therefore, it is a matter of design choice as to which one is used." (*See* Office Action, pgs. 8-9)

Applicant respectfully asserts that Claim 12 is not obvious in view of the combination of Douceur and Mano et al. Douceur does not anticipate the method of claim 1 as indicated above with respect to claim 1, and Mano et al. does not cure this defect. Thus, Applicant respectfully asserts that the references, alone or in combination, do not teach or suggest the claimed invention.

Therefore, based on the above arguments, it is respectfully requested that the rejection of claim 12 be withdrawn.

Claim 25

Claim 25 depends from independent claim 14. As a result, the arguments presented above with respect to claim 14 apply to this claim as well.

Applicant refers the Examiner to the arguments presented above with respect to claim 12. Accordingly, it is respectfully requested that the rejection of claim 25 be withdrawn.

Allowable Subject Matter

Claims 2-6, 9, 11, 15-19, 22, and 24 were objected to as being dependent upon a rejected base claim, but were indicated to be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. In view of the terminal disclaimer discussed above, applicant respectfully asserts that these claims are allowable without amendment. Withdrawal of the objection is respectfully requested.

CONCLUSION

Applicant respectfully submits that claims **1-6, 9-19, and 22-26** are in condition for allowance and notification to that effect is earnestly requested. If necessary, please charge any additional fees or credit overpayments to Deposit Account No. 502432.

If the Examiner has any questions or concerns regarding this application, please contact the undersigned at the telephone number listed below.

Respectfully submitted,

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David N. Fogg
Reg. No. 35,138

Attorneys for Applicant
Fogg & Associates, LLC
P.O. Box 581339
Minneapolis, MN 55458-1339
T – (612) 332-4720
F – (612) 332-4731